Solutions - Quiz 2
(October 8th @ 5:30 pm)

PROBLEM 1 (40 PTS)
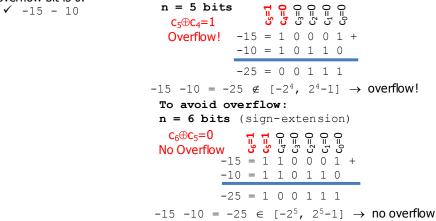
▪ Complete the following table. Use the <u>fewest</u> number of bits in each case:

REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
−3	111	100	101
−7	1111	1000	1001
−2	110	101	10
2	010	010	010

▪ Convert the following decimal number to its 2's complement representation: −8.75 (5 pts)

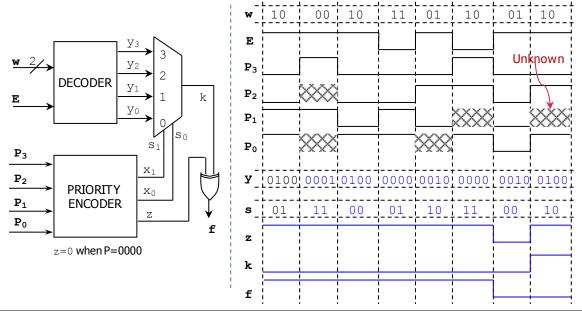$8.75 = 01000.11_2 \rightarrow -8.75 = 10111.01_2$

PROBLEM 2 (20 PTS)

▪ Perform the following operation in the 2's complement representation, i.e., provide the summands and the result in 2's complement representation. Use the minimum number of bits to represent both the summands and the result so that the overflow bit is 0.

✓ −15 − 10

```
n = 5 bits          c₅=1  c₄=0  c₃=0  c₂=0  c₁=0  c₀=0
c₅⊕c₄=1
Overflow!   -15 =  1  0  0  0  1 +
            -10 =  1  0  1  1  0
                 ─────────────────
            -25 =  0  0  1  1  1
```

$-15 - 10 = -25 \notin [-2^4, 2^4-1] \rightarrow$ overflow!

To avoid overflow:
n = 6 bits (sign-extension)

```
c₆⊕c₅=0            c₆=1  c₅=1  c₄=0  c₃=0  c₂=0  c₁=0  c₀=0
No Overflow
            -15 =  1  1  0  0  0  1 +
            -10 =  1  1  0  1  1  0
                 ────────────────────
            -25 =  1  0  0  1  1  1
```

$-15 - 10 = -25 \in [-2^5, 2^5-1] \rightarrow$ no overflow

PROBLEM 3 (40 PTS)

▪ Complete the timing diagram of the circuit shown below: